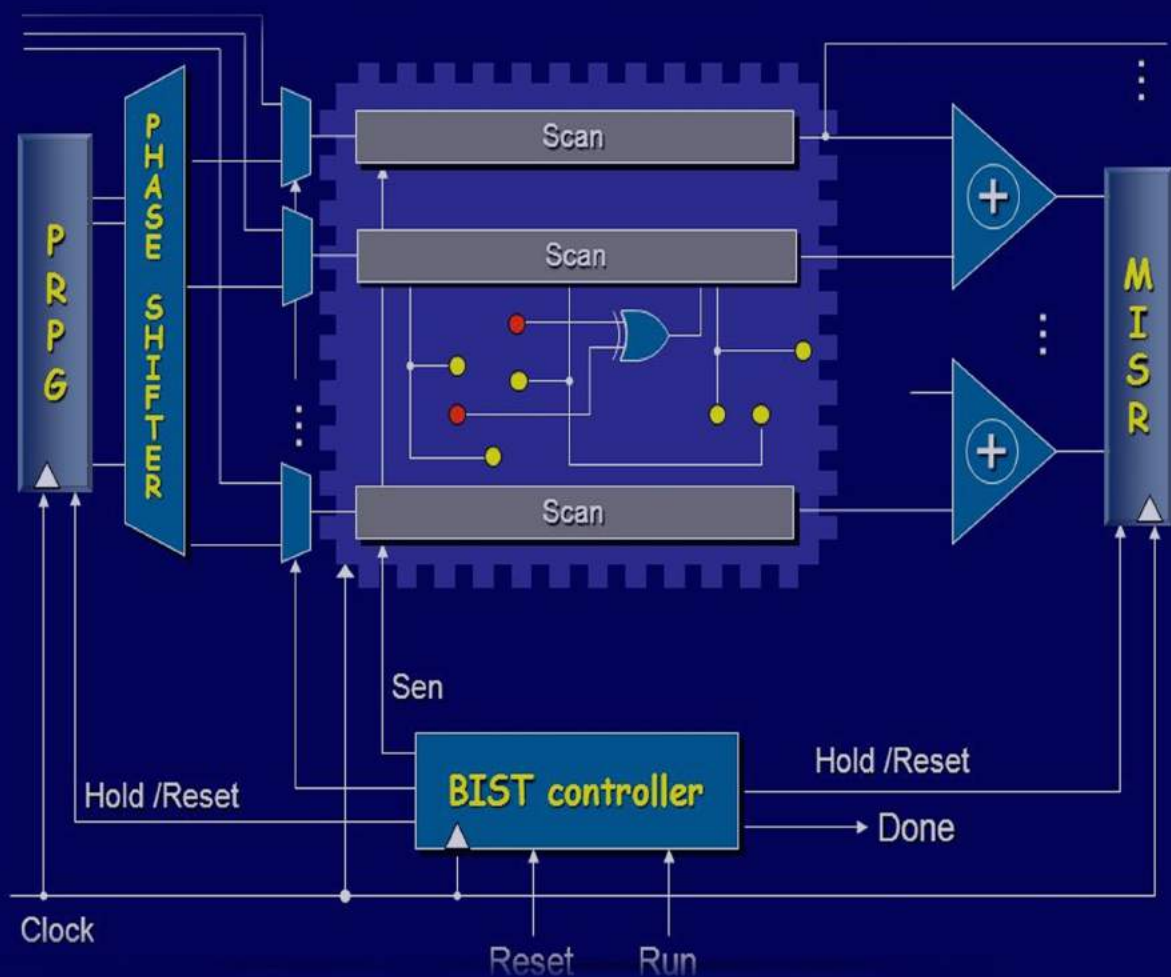


A Handbook on Design and Analysis of Novel Concurrent Cellular Automation Logic Block Observer BIST Structure



Er. Ravi Trivedi
Dr. Sandeep Dhariwal
Dr. Ravi Shankar Mishra
Dr. Rajkumar Sarma



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Authors

Er. Ravi Trivedi

Dr. Sandeep Dhariwal

Dr. Ravi Shankar Mishra

Dr. Rajkumar Sarma



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Er. Ravi Trivedi, Member of senior technical staff, Digicomm Semiconductors Pvt. Ltd., Pune

Dr. Sandeep Dhariwal, Associate Professor, ECE, Alliance College of Engineering and Design, Alliance University, Bengaluru, Karnataka.

Dr. Ravi Shankar Mishra, Professor & Head, Department of Electronics & Communication Engineering, Sagar Institute of Science & Technology (SISTec) Bhopal (M.P.) 462 036.

Dr. Rajkumar Sarma, Assistant Professor, EEE Department, FET, Jain (Deemed-to-be-University), Bangalore.

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Dedicated
to
Almighty God

Preface

An efficient Design for Testability (DFT) has been a major concern for today's VLSI engineers. A poorly designed DFT would result in losses for manufacturers with a considerable rework for the designers. Built-in Self-Test (BIST) – One of the promising DFT techniques is rapidly modifying with the advances in technology as device shrinks. Because of the growing complexities of the hardware, the trend has shifted to include BISTs in high performance circuitry for offline as well as online testing. Work done here involves testing various Circuit Under Test (CUT) with different techniques of built in response analyzer and vector generator with a monitor to control all the activities. Use of low transition vector generators like Bit-Swapping Complete Feedback Shift Register (BS-CFSR), Cellular Automata Registers (CAR), Concurrent Built-In Logic Block Observer (CBILBO), and, novel design Concurrent Cellular Automata Logic Block Observer (CCALBO) an effort is made to reduce power consumption by comparing it to classical Linear Feedback Shift Register (LFSR) techniques. This book presents the process of design implementation for a complete BIST working on both normal operation mode as well as test mode for multiple circuitry like Carry Look Ahead (CLA) adder, ISCAS benchmark circuits (74XX series) – 74181 and 74283, Vedic Multiplier, and Multiply and Accumulate processor. A thorough comparison is carried out by comparing all the DFT techniques with each other. *Xilinx Vivado 2018.1* for coding in Verilog and implementation with *Cadence's Encounter(R) RTL Compiler RC 14.10* were used for timing responses, area calculations, and power consumption at different technology nodes.

Er. Ravi Trivedi
Dr. Sandeep Dhariwal
Dr. Ravi Shankar Mishra
Dr. Rajkumar Sarma

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Last but not least, we also convey our deepest gratitude to our parents for whose faith, patience and teaching had always inspired us to walk upright in our life.

Finally, we humbly bow our head with utmost gratitude before the God Almighty who always showed us a path to go and without whom we could not have done any of these.

Er. Ravi Trivedi
Dr. Sandeep Dhariwal
Dr. Ravi Shankar Mishra
Dr. Rajkumar Sarma

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About the Authors



Mr. Ravi Trivedi received his M.Tech degree from Lovely Professional University (Punjab). He has published several research papers in reputed conferences and journals. At present, he is working as senior technical staff member in Digicomm Semiconductors Pvt. Ltd., Pune in the field of Broadcom Inc. client. His area of research includes Physical Verification, VLSI Testing, STA.



Dr. Sandeep Dhariwal received his B.E. in 2004 from C.R.S.C.E. Murthal (M.D.U. Rohtak) in ECE. He completed his M.Tech from G.J.U.S.T. Hisar in 2008 in VLSI Design and Embedded Systems. He completed his Ph.D. in 2015 from Banasthali University- Banasthali (Rajasthan) in Electronics Engineering. Currently he is working as an associate professor in ACED, Alliance University (central Campus) Bengaluru (INDIA). His area of research includes low power VLSI design, Testing of VLSI circuits, Digital VLSI Design. He has published many research articles in reputed national and international journals and conferences.



Dr. Ravi Shankar Mishra has received his Ph.D. in 2011 and M.Tech. in 2005 from N.I.T. Bhopal. He has completed his PG Diploma in VLSI Design from C-DAC Bangalore. He has 19+ years of research and academic experience in reputed institutions such as Lovely Professional University (LPU) Punjab, Symbiosis University of Applied Sciences (SUAS), Indore, Guru Nanak Institute of Technology (GNIT) Hyderabad. He has handled the important position of responsibilities like Dean, Head of Department, Research Coordinator, etc. He has published more than 40 research papers in reputed international journals and international conference proceedings including SCI, Scopus. He is also a reviewer of many Journals. One copyright and two books are registered with his name. He has supervised 3 Ph.D. scholars and 18 dissertations at the PG level. He is a Life Fellow Member of the Institution of Electronics & Telecommunication Engineers (IETE) and International Association of Engineers (IAENG). His research contributions have been in the area of designing efficient PUF based circuits to using CMOS for generating the secure key.



Dr. Rajkumar Sarma received his B.E. in Electronics and Communications Engineering from Vinayaka Mission's University, Salem, India in 2008. He received his M.Tech as well as Ph.D. degrees from Lovely Professional University, Phagwara, Punjab in the years 2012 & 2020 respectively. He is working as an Assistant Professor (Senior Grade) in the School of Electrical and Electronics Engineering, Jain (Deemed - To- Be - University), Ramanagara, Karnataka. His research interests include Analog and Digital VLSI design, Prototype development using FPGA etc. The author has around 20+ research publications in SCI/Scopus indexed reputed Journals and national/international Conferences. Moreover, the author has 15+ patents/copyrights published in various engineering fields. He has also authored and edited several books and book chapters from reputed publishers.



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